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Design of FinFET Based 4-Bit Input XOR & XNOR Logic Circuit

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ABSTRACT- A design for direct 4-BIT XOR&XNOR logic circuit is proposed by using pass transistor logic with FinFET transistors. The simulation results illustrate that the proposed design has high speed and as well as less power consumption when compared to planar devices.

I. INTRODUCTION

FinFETmeans MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is having more than one gates in the transistor. Which is controlled by a single gate electrode and also it is Silicon-on-Insulator (SI) based transistor. When the conducting channel increases above the level of insulator, then it will form thin silicon structure. It is called as Fin. Hence the transistor is called as FinFET. Hence it was developed by Chenming Hu from California at the University of Berkley.



Fig 1 (a) Top view of doublegate FinFET structure



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Fig.1 (b) p-FINFET and n-FINFET

Therefore, the need of using FinFET transistor is while moving to scale down the transistor will bring up a short channel effect and a static power dissipation in it. In order to overcome this demerit from the planar transistors we using the FinFET transistors. Thus the FinFET transistor have a good channel control in it. Due to that it will work faster than any other planar devices.

II. RELATED WORK

In our design, the supply voltage is decreased to bring down the power dissipation. FinFET consists of Front-Gate and Back-Gate in which the gates are surrounded around as to reduce the leakage of current.



Fig.2 Circuit diagram for proposed design

During the forward bias the currents flows through Drain-source (I_{ds}) . The leakage of charges is reduced to maximum extent. And the P-FinFET will go low and the N-FinFET will go high. Its operation is similar to MOSFET. But, designing of a XOR and EXNOR logic circuits requires a large number of transistors while considering a Pass-Transistor Logic (PTL). But, in FinFET while we design logic with planar MOSFET we get



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lot of leakage charges. XOR and EXNOR logic gates are used in day to day electronics. So with the help of FinFET we can reduce the power dissipation and scaling of transistor will be convenient.

In the proposed method 4 input XOR/XNOR structure can be better analyzed by considering the complete set of input signals ABCD = 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111. For example, in Fig. 2, for '0000' combination of inputs the transistors T1, T2, T3, T4, T5, T6, T8 and T9 are switched ON so that the full logic '0' to XOR output and full logic '1' is produced at the EXNOR output through the inverter. When an input pattern is '0001', the transistors T1, T2, T3, T4, T7 and T10 are switched ON that degraded logic '1' is generated at XOR output, then the transistors in the inverters to give EXNOR output. For ABCD = '1101', then the transistors T2, T4 and T7 p2 are switched ON and input D i.e. full logic '0' is passed to the output of EXNOR and full logic '1' is generated at the output XOR through inverter I. For ABCD= '1100', then the transistors T3, T4, T7 and T10 are switched ON to get logic '1' and EXNOR logic willbe '0'. A similar operation applies to the rest of the cases.

The Advantages for the proposed method are

1) Faster switching speed.(comes from lower input higher dynamic current).

2) Lower power consumption (comes from lower parasitic capacitance and better on/off characteristics). From the physicist's perspective:

3) Channel quantization, reducing short-channel effects.

III. SIMULATION RESULTS

A 4Bit-input XOR/EXNOR circuit shown in Fig. 3 and it is simulated using Cadence Virtuoso 22 nm FinFET technology at supply voltages ranging is +0.6. Because of using a PTL logic with FinFET transistors. When compared to planar circuits the proposed gives less propagation delay and dynamic power dissipation.



Fig 3 Input and output waveforms for 4-input XOR/XNOR logic Circuit

IV. CONCLUSION

The design is proposed for 4-BIT input XOR&EXNOR logic circuit with minimum number of transistors by using pass transistor ogic with FinFET transistors. The simulation results prove that the circuit hasless delay with high speed as well as lesspower consumption.

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